IN THE CLAIMS

Re-write Claims 19 and 21, 27, 32, 36 and 38. Cancel Claims 20, 26 and 33.

1. (previously withdrawn) A method of forming a conductive strap in a semiconductor device, the method comprising:

forming a semiconductor structure including a source/drain region located in a substrate, a gate located over the source/drain region, and a dielectric spacer located over the source/drain region and adjacent to the gate;

implanting a semiconductor material into upper surfaces of the gate, the dielectric spacer, and the source/drain region;

depositing a refractory metal over the implanted semiconductor material; and

reacting the refractory metal with the implanted semiconductor material, thereby forming a continuous metal silicide strap at the upper surfaces of the gate, the dielectric spacer and the source/drain region.

2. (previously withdrawn) The method of Claim 1, wherein the step of implanting a semiconductor material comprises implanting silicon.

3. (previously withdrawn) The method of Claim 1, wherein the step of depositing a refractory metal comprises sputter depositing cobalt.

4. (previously withdrawn) The method of Claim 1, wherein the step of reacting the refractory metal comprises annealing at a temperature of 800°C or greater.

5. (previously withdrawn) The method of Claim 1, further comprising the steps of:

forming a silicon-blocking layer over the semiconductor structure;

patterning the silicon blocking layer to form an opening which exposes a portion of the gate, the dielectric spacer and a portion of the source/drain region; and

implanting the semiconductor material through the opening.

6. (previously withdrawn) The method of Claim 5, wherein the implanting step is performed at an angle with respect to the opening.

7. (previously withdrawn) The method of Claim 5, wherein the refractory metal is deposited over the patterned silicon blocking layer and into the opening.

8-18. (previously cancelled)

19. (presently amended) A semiconductor structure comprising:

a semiconductor substrate;

a conductive element located over the semiconductor substrate;

a dielectric spacer located adjacent to a sidewall of the conductive element, wherein an upper surface of the dielectric spacer is silicon-rich, and a portion of the dielectric spacer, located away from the upper surface of the dielectric spacer, is not silicon-rich; and

a continuous refractory metal layer ~~silicide strap~~ directly contacting the conductive element, the dielectric spacer and the semiconductor substrate.

20. (canceled) The semiconductor structure of Claim 19, wherein a portion of the dielectric spacer, located away from the upper surface of the dielectric spacer, is not silicon-rich.

21. (presently amended) A semiconductor structure comprising:

a semiconductor substrate;

a conductive element located over the semiconductor substrate;

a dielectric spacer located adjacent to a sidewall of the conductive element;

a semiconductor region dispersed in the upper surfaces of the conductive element, the dielectric spacer and the semiconductor substrate; and

a continuous refractory metal layer located directly on ~~silicide strap formed in~~ the semiconductor region.

22. (previously added) The semiconductor structure of Claim 21, wherein the dielectric spacer is silicon-rich.

23. (previously added) The semiconductor structure of Claim 21, wherein the semiconductor region comprises amorphous silicon.

24. (previously added) The semiconductor structure of Claim 21, wherein the semiconductor region comprises an implanted semiconductor layer.

25. (previously added) The semiconductor structure of Claim 24, wherein the implanted semiconductor layer comprises silicon.

26. (canceled) The semiconductor structure of Claim 19, wherein the silicide strap comprises a refractory metal layer reacted with semiconductor material in the conductive element, the dielectric spacer and the semiconductor substrate.

27. (presently amended) The semiconductor structure of Claim 26, wherein the refractory metal layer directly contacts ~~semiconductor material comprises~~ amorphous silicon in the conductive element, the dielectric spacer and the semiconductor substrate.

28. (previously added) The semiconductor structure of Claim 19, wherein the conductive element is a gate electrode.

29. (previously added) The semiconductor structure of Claim 28, further comprising a gate dielectric layer located between the semiconductor substrate and the gate electrode.

30. (previously added) The semiconductor structure of Claim 19, further comprising a source/drain region located in the semiconductor substrate, wherein the refractory metal layer ~~silicide strap~~ contacts the source/drain region.

31. (previously added) The semiconductor structure of Claim 19, wherein the dielectric spacer comprises silicon oxide or silicon nitride.

32. (presently amended) The semiconductor structure of Claim 19, wherein the refractory metal layer ~~silicide strap~~ comprises cobalt ~~silicide~~.

33. (canceled) The semiconductor structure of Claim 21, wherein the silicide strap comprises a refractory metal layer reacted with the semiconductor region.

34. (previously added) The semiconductor structure of Claim 21, wherein the conductive element is a gate electrode.

35. (previously added) The semiconductor structure of Claim 34, further comprising a gate dielectric layer located between the semiconductor substrate and the gate electrode.

36. (presently amended) The semiconductor structure of Claim 21, further comprising a source/drain region located in the semiconductor substrate, wherein the refractory metal layer ~~silicide strap~~ contacts the source/drain region.

37. (previously added) The semiconductor structure of Claim 21, wherein the dielectric spacer comprises silicon oxide or silicon nitride.

38. (presently amended) The semiconductor structure of Claim 21, wherein the refractory metal layer ~~silicide strap~~ comprises cobalt ~~silicide~~.

39. (previously added) The semiconductor structure of Claim 21, wherein the upper surface of the dielectric spacer is silicon-rich, and wherein a portion of the dielectric spacer, located away from the upper surface of the dielectric spacer, is not silicon-rich.